AMENDMENTS TO THE CLAIMS

Claims 1, 2, 3, 9, 13, 16, 24, 25, 29, 33, and 36-38 have been amended, claims 7, 12, 14, 15, 19, 28, 30, and 31 have been cancelled, and claims 39-46 have been added. The following is a complete listing of the claims, which replaces all previous versions and listings of the claims.

1. (currently amended) A method for transacting between an initiator device and a plurality of target devices, the method comprising:

configuring the plurality of target devices to recognize a single base address ~~associate a portion of memory with a particular target device of the plurality of target devices~~;

sending a multicast transaction from the initiator device to the plurality of target devices, wherein sending the multicast transaction comprises sending a multicast transaction to the single base address associated with each of the plurality of target devices; and

executing the transaction when the transaction is received by the plurality of target devices according to the configuration of the target device.

2. (previously presented) The method of claim 1, comprising:

assigning a base memory address to be shared by the plurality of target devices; and

assigning a first portion of memory to a first target device of the plurality of target devices.

3. (currently amended) The method of claim 2, wherein the transaction is a read request for a block of stored data from memory, comprising:

recognizing ~~reading~~ the base memory address from the read request;

initiating a read operation by the plurality of target devices assigned to the base memory address;

fetching stored data from a portion of memory associated with each of the target devices, the data being concurrently fetched by each associated target device; and

sending the fetched data to the initiator device.

4. (currently amended) The method of claim 2, wherein the transaction is a write request for data to be stored in memory, comprising:

recognizing ~~reading~~ the base memory address from the write request;

initiating a write operation by the plurality of target devices assigned to the base memory address; and

writing data of the write request to a portion of memory associated with each target device, the data being concurrently written by each associated target device.

5. (original) The method of claim 1, wherein the target devices comprise input/output controllers.

6. (original) The method of claim 1, wherein the target devices comprise disk array controllers.

7. (cancelled)

8. (previously presented) The method of claim 1, comprising a plurality of target groups.

9. (currently amended) A method for transacting data stored in memory between an initiator device and multiple target devices, the method comprising:

detecting a multicast transaction request;

accessing a first portion of memory by a first target device in response to the multicast transaction request; and

accessing a second portion of memory by a second target device concurrently with the access to the first portion of memory in response to the multicast transaction request, wherein the first and second portions of memory are accessed with a single base address associated with the first target device and the second target device.

10. (original) The method of claim 9, wherein the target devices comprise input/output controllers.

11. (original) The method of claim 9, wherein the target devices comprise disk array controllers.

12. (cancelled)

13. (currently amended) The method of claim 9, comprising accessing a plurality of target devices, wherein the plurality of target devices are divided ~~configured~~ into ~~multiple target~~ a plurality of groups, wherein each of the ~~multiple target~~ plurality of groups is ~~addressable with a single base memory address~~ associated with a single base memory address configured to address the target devices within that group.

14-15. (cancelled)

16. (currently amended) A computer system ~~for communicating between an initiator device and multiple target devices~~ comprising:

a ~~communications~~ bus;

an initiator device coupled to the ~~communications~~ bus, the initiator device configured to initiate a transaction request; and

a plurality of target devices coupled to the ~~communications~~ bus, wherein each of the plurality of target devices concurrently executes a portion of the transaction request, wherein the initiator device is configured to multicast a transaction

request to the plurality of target devices using a single base address associated with the plurality of target devices.

17. (previously presented) The computer system of claim 16, wherein the plurality of target devices comprise input/output controllers.

18. (previously presented) The computer system of claim 16, wherein the plurality of target devices comprise disk array controllers.

19. (cancelled)

20. (original) The computer system of claim 16, wherein the plurality of target devices comprise a target group.

21. (previously presented) The computer system of claim 20, comprising a plurality of target groups.

22. (original) The method of claim 16, wherein the transaction is a multicast read request.

23. (original) The method of claim 16, wherein the transaction is a multicast write request.

24. (currently amended) The computer system of claim 16, wherein the ~~communications~~ bus comprises a Peripheral Component Interconnect (PCI) bus.

25. (currently amended) A computer system ~~for multicast input/output transactions,~~ comprising:

a processor;

a ~~communications~~ bus coupled to the processor;

an initiator device coupled to the ~~communications~~ bus, the initiator device configured to issue a multicast transaction; and

a plurality of target devices coupled to the ~~communications~~ bus, the plurality of target devices configured to execute the multicast transaction with concurrent ~~interleaved~~ data responses from a plurality of interleaved memory regions, wherein the initiator device is configured to multicast the transaction request to the plurality of target devices using a single base address associated with the plurality of target devices.

26. (original) The computer system of claim 25, wherein the target devices comprise input/output controllers.

27. (original) The computer system of claim 25, wherein the target devices comprise disk array controllers.

28. (cancelled)

29. (currently amended) The computer system of claim 28, wherein the plurality of target devices are divided into a plurality of target groups, wherein each of the target groups is associated with its own base address ~~comprising a plurality of target groups~~.

30-31. (cancelled)

32. (previously presented) A computer comprising:

a memory;

a controller configured to logically divide the memory into a plurality of interleaved memory regions; and

a plurality of devices, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction request.

33. (currently amended) A method comprising:

dividing a section of memory into a plurality of interleaved memory regions;

associating the plurality of interleaved memory regions with a plurality of target devices;

associating the plurality of target devices with a single base memory address; and

executing a memory access using the single base memory address ~~that simultaneously involves each of the plurality of target devices accessing the interleaved memory region associated with each of the particular target devices~~.

34. (previously presented) The method of claim 33, wherein executing the memory access comprises executing a read operation.

35. (previously presented) The method of claim 33, wherein executing the memory access comprises executing a write operation.

36. (currently amended) A tangible machine readable medium comprising:

code to initialize a plurality of devices;

code to configure the plurality of devices to associate a single base address with the plurality of devices; and

code to associate the single base address with a plurality of interleaved memory regions ~~code to assign each of the plurality of devices a portion of an interleaved memory space~~.

37. (currently amended) The tangible medium of claim 36, comprising:

code to issue a single read command comprising the single base address;

code to recognize the single base address as associated with the plurality of devices;

code to simultaneously execute a plurality of memory requests involving the plurality of devices;

code to receive data from the plurality of devices; and

code to write the received data to a ~~communications~~ bus.

38. (currently amended) The tangible medium of claim 36, comprising:

code to issue a write command comprising the single base address;

code to recognize the base address as associated with the plurality of devices; and

code to simultaneously write to the plurality of devices.

39. (new) The method of claim 1, wherein sending the multicast transaction comprises sending the multicast transaction from a disk drive controller to a plurality of disk drives.

40. (new) The method of claim 1, wherein sending the multicast transaction comprises sending the multicast transaction from a SCSI controller to a plurality of SCSI devices.

41. (new) The computer system of claim 16, wherein the initiator device comprises a SCSI controller.

42. (new) The computer system of claim 16, wherein the plurality of target devices comprises a plurality of disk drives.

43. (new) The computer system of claim 25, wherein the initiator device comprises a SCSI controller.

44. (new) The computer system of claim 25, wherein the plurality of target devices comprises a plurality of SCSI hard drives.

45. (new) The computer of claim 32, wherein the controller comprises a SCSI controller.

46. (new) The computer of claim 32, wherein the plurality of devices comprises a plurality of SCSI hard drives.